Amendments to the Specification:

Please replace the paragraph at page 1, lines 26-31 with the following amended paragraph:

FIG. 1 is a view of a X4 data input/output format, and FIG. 2 is a view of a conventional circuit for transforming a data input/output format from a X4 mode to a X2 mode. If the number of memory cells (MC), e.g., MC1, MC2, MC4, MC5, ~~MC0-MC5~~ connected to a column select line CSL is equal to the number of data input pins DIN0-DIN3, no problems occur. That is, all types of data patterns can be tested by writing and reading the data patterns to and from four memory cells MC1, MC2, MC4, MC5, ~~MC0-MC5~~ while using four data input pins DIN0-DIN3.

Please replace the paragraph at page 2, lines 1-6 with the following amended paragraph:

However, in the circuit of FIG. 2, two memory cells are connected to one data input pin through a circuit 20 for transforming a data input/output format. That is, two memory cells MC0 and MC1 are connected to a data input pin DIN0, and two memory cells MC4 and MC5 are connected to a data input pin DIN1. As a result, the number of memory cells MC0, MC1, MC4, MC5 ~~MC0-MC5~~ connected to one column selection line CSL is greater than the number of data input pins DIN0 and DIN1.

Please replace the paragraph at page 2, lines 7-9 with the following amended paragraph:

In this case, the types of data patterns that can be written to the memory cells MC0-MC5 are limited. The following Table 1 shows types of data patterns that can be written to the memory cells MC1, MC2, MC4, MC5 ~~MC0-MC5~~ in the circuit of FIG. 2.

Please replace the paragraph at page 4, line 28 through page 5 line 2 with the following amended paragraph:

The first transmission circuit 31 is activated when a first test mode signal PBTX2_SS is enabled as logic high, receives two data inputs from two data input ends DIN0 and DIN1, and transmits the data inputs to four memory cells (MC) MC0, MC1, MC4, and MC5. The second transmission circuit 32 is activated when a second test mode signal PBTX2_DS is enabled as logic high, receives two data inputs from two data input ends DIN0 and DIN1, and transmits the data inputs to four memory cells MC0, MC1, MC4, and MC5. Here, a signal PCLKM is maintained as logic high.